EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	11335	(logic near4 gate) and (flash near4 memory)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/22 11:06
L2	3	(hardmask near9 (logic near4 gate)) and (hardmask near9 (flash near4 memory))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/22 11:08
L3	58	(mask near9 (logic near4 gate)) and (mask near9 (flash near4 memory))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/22 11:08
L4	22	(mask near9 (logic near4 gate)) and (mask near9 (flash near4 memory)) and (pattern near9 mask)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/22 11:09
L5	21	(mask near9 (logic near4 gate)) and (mask near9 (flash near4 memory)) and (pattern near9 mask) and (pattern near9 gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/22 11:09
L6	20	(mask near9 (logic near4 gate)) and (mask near9 (flash near4 memory)) and (pattern near9 mask) and (pattern near9 gate) and (etch$4 near9 gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/22 11:35
L7	2	(mask near9 (logic near4 gate)) and (mask near9 (flash near4 memory)) and (pattern near9 mask) and (pattern near9 gate) and (etch$4 near9 gate) and (438/257.ccls.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/22 11:36

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S1	0	(logic near gate) and stack and region and (substrate or wafer or semiconductor) and (flash near memory) and (deposit near8 hardmask) and pattern$4 and etch$4 and die and dielectric and electrode and float$4 and control and (ARC or "anti-rflective coating") and pitch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:27
S2	0	logic and stack and region and (substrate or wafer or semiconductor) and (flash near memory) and (deposit near8 hardmask) and pattern$4 and etch$4 and die and dielectric and electrode and float$4 and control and (ARC or "anti-rflective coating") and pitch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:27
S3	0	logic and stack and region and (substrate or wafer or semiconductor) and (flash near memory) and (deposit near8 hardmask) and pattern$4 and etch$4 and die and dielectric and electrode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:27
S4	0	logic and stack and region and (substrate or wafer or semiconductor) and (flash near memory) and (deposit near8 hardmask) and pattern$4 and etch$4 and die	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:27
S5	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and (deposit near8 hardmask) and pattern$4 and etch$4 and die	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:28
S6	26	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:28
S7	23	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:28

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S8	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode and (ARC or "anti-reflective coating")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:29
S9	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode and (ARC or "anti reflective coating")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:29
S10	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode and ARC	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:29
S11	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode and reflective	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:29
S12	23	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:00
S13	38	flash adj logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:01
S14	1	flash adj logic and hardmask and pattern$4 and etch$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:02

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S15	1	flash adj logic and hardmask	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:02
S16	6	flash adj logic and (ARC or "anti-reflective coat$4")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:03
S17	3	flash adj logic and (ARC or "anti-reflective coat$4") and pattern	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:03
S18	3	flash adj logic and (ARC or "anti-reflective coat$4") and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:03
S19	3	flash adj logic and (ARC or "anti-reflective coat$4") and pattern and etch and (substrate or semicondcutor or wafer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 12:41
S20	3	flash adj logic and (ARC or "anti-reflective coat$4") and pattern and etch and (substrate or semicondcutor or wafer) and resist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 12:48
S21	0	flash adj logic and (ARC or "anti-reflective coat$4") and pattern and etch and (substrate or semicondcutor or wafer) and resist and float	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 13:00
S22	12	logic and flash and substrate and memory and "ARC" and (resist near4 resist) and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 11:36

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S23	1	("logic gate" near8 (stack near4 region)) and ((flash near memory) near4 region) and (substrate or semiconductor or wafer) and (hardmark or "ARC") and (flash near4 gate) and (pattern$4 or etch$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 11:42
S24	243	((etch near4 "logic gate") near8 hardmask or "ARC") and (flash near memory) and stack and (substrate or semiconductor or wafer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 11:53
S25	16	((etch near4 "logic gate") near8 hardmask or "ARC") and (flash near memory) and stack and (substrate or semiconductor or wafer) and (logic near4 region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 11:54
S26	15930	logic and flash and (NAND or NOR)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:01
S27	8640	logic and flash and (NAND or NOR) and (semiconductor or substrate or wafer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:01
S28	31	logic and flash and (NAND or NOR) and (semiconductor or substrate or wafer) and hardmask	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:01
S29	22	(logic near4 gate) and flash and (NAND or NOR) and (semiconductor or substrate or wafer) and hardmask	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:04
S30	13	(logic near4 gate) and flash and (NAND or NOR) and (semiconductor or substrate or wafer) and hardmask and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:11

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S31	1	(logic near4 gate) and (flash near4 gate) and (NAND or NOR) and (semiconductor or substrate or wafer) and hardmask and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:13
S32	12	(logic near4 gate) and (flash near4 memory) and (NAND or NOR) and (semiconductor or substrate or wafer) and hardmask and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:13
S33	25	(logic near4 gate) and (flash near4 memory) and (semiconductor or substrate or wafer) and hardmask and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:16
S34	1	(logic near4 gate) adj (flash near4 memory) and (semiconductor or substrate or wafer) and hardmask and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:17
S35	0	(logic near4 gate) adj (logic near4 gate) and (semiconductor or substrate or wafer) and hardmask and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:18
S36	4	"6235587"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:22
S37	0	"6235587" and "6417086"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/06 11:22
S38	4	(("6235587") or ("6417086")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2006/05/01 11:27

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S39	2	"6376312".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/01 11:27